What is claimed is:

1. A method of fabricating a semiconductor device, comprising the steps of:

sequentially forming an insulating material layer and an anti-etch film on the entire semiconductor substrate;

making the anti-etch film and the insulating material layer remained only in an isolation region through an etch process, thus forming a device isolation film made of an insulating material layer; and

forming an active region layer where the semiconductor device will be formed between the device isolation films.

2. The method as claimed in claim 1, wherein the anti-etch films are made of a silicate film or a silicon nitride film.

3. The method as claimed in claim 2, wherein the silicate film is made of $AlSi_xO_y$, $HfSi_xO_y$, YSi_xO_y, $CeSi_xO_y$ or $TaSi_xO_y$, or a mixture of at least more than one of them.

4. The method as claimed in claim 3, wherein the composition ratio X is $0.05 \sim 10$ and the composition ratio Y is $0.05 \sim 10$.

5. The method as claimed in claim 1, further comprising the step of before the etch process is implemented after the anti-etch film is formed or

before the active region layer is formed after the etch process is performed, implementing an annealing process under an atmosphere of N_2, O_2, O_3, H_2, D_2, H_2O, D_2O, NO, N_2O or a mixed gas of them at a temperature of 600 ~ 1000℃ for 20 seconds ~ 60 minutes.

6. The method as claimed in claim 1, wherein the active region layer is formed by means of a selective epitaxial growth process and is formed by growing a silicon layer, a silicon-germanium layer, or the silicon layer after the silicon-germanium layer is grown.

7. The method as claimed in claim 6, wherein in the selective epitaxial growth process, SiH_4 or SiH_2Cl_2 and Cl_2 gases are used as a reaction gas.

8. The method as claimed in claim 1, further comprising the steps of after the active region layer is formed,

removing the active region layer that is formed higher than the device isolation film, by means of a chemical mechanical polishing process; and

implementing an annealing process in order to mitigate polishing damage and improve an interfacial characteristic between the device isolation film and the active region layer.

9. A method of fabricating a semiconductor device, comprising the steps of:

sequentially forming an insulating material layer and a high dielectric insulating film on the entire semiconductor substrate;

making the high dielectric insulating film and the insulating material layer remained only in an isolation region through an etch process, thus forming a device isolation film made of an insulating material layer; and

excessively growing an active region layer containing silicon on the semiconductor substrate between the device isolation films by means of a selective epitaxial growth process, whereby the active region layer is formed up to the top corner of the high dielectric insulating film, and anti-etch films are formed at the top corners of the device isolation film through reaction of silicon components of the active region layer and the high dielectric insulating film.

10. The method as claimed in claim 9, wherein the high dielectric insulating film is formed using Al_2O_3, HfO_2, ZrO_2, Y_2O_3, CeO_2, Ta_2O_5 or a mixture of them.

11. The method as claimed in claim 9, wherein the anti-etch film is formed using a silicate film.

12. The method as claimed in claim 9, wherein the active region layer is formed by means of a selective epitaxial growth process and is formed by growing a silicon layer, a silicon-germanium layer, or the silicon layer after the silicon-germanium layer is grown.

13. The method as claimed in claim 12, wherein in the selective epitaxial growth process, SiH_4 or SiH_2Cl_2 and Cl_2 gases are used as a reaction gas.

14. The method as claimed in claim 9, further comprising the steps of after the active region layer is formed,

removing the active region layer that is formed higher than the device isolation film, by means of a chemical mechanical polishing process; and

implementing an annealing process in order to mitigate polishing damage and improve an interfacial characteristic between the device isolation film and the active region layer.